

REMARKS

Figures 6A to 9B are all designated with the label "Prior Art".

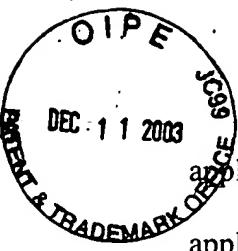
With regard to the prior art disclosed in the referenced application, the conventional memory testing method is implemented in such way that all memory addresses, one by one are **CONTINUOUSLY** detected to test whether the detected memory addressed is a weakened one.

Based on the presently amended claims 1-3 and new claims 11-13, the memory test method is performed by two main steps. In the first step, accessing commands are applied to test a first group of the memory address consisting of even rows, for example. After the first step is finished, the second step starts to perform accessing commands to test a second group of the memory address that are complementary to the first group of memory addresses, i.e. odd rows. It is noted that the testing order for memory addresses is interlaced and different from the prior arts.

With reference to amended Claim 4, applicants recites a method in which a testing program is executed to perform an interlace memory testing.

With regard to the cited reference U.S. 4,513,374, Hooks, Jr. teaches "when the frame buffer is read, the start address is generated. . . in such a way as to produce interlaced. . ." fields requiring "sequence. . . for even fields and for odd fields, so data is repeated for even and odd fields". However, the disclosure of Hooks, Jr. is related to an image generating technique **not the memory testing field**.

For one skilled in the memory testing art, the image generating technique is not so familiar. Therefore, how to combine the two different techniques is still a problem. Based on such reason,



applicant asserts that the rejection under 35 U.S.C. 103(a) should be withdrawn and the application is patentable over the cited prior art. Thus, an early granting of the application is respectfully requested. Replacement drawings sheets will be submitted upon the issue of a Notice of Allowance.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited on the date shown below with the United States Postal Service, with sufficient postage as First Class Mail (37 CFR 1.8(a)), in an envelope addressed to Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

Date: December 8, 2003

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